CLAIMS

What is claimed is:

1. A flip chip package, comprising an integrated circuit chip having interconnect bumps formed on input/output pads in a specified arrangement, and a package substrate having a plurality of bond pads in a complementary arrangement, wherein interconnection between the bumps on the integrated circuit chip and the respective bond pads on the package substrate is established by direct mating of the bump surfaces with the respective bond pads and thermo-mechanical deformation of the bumps.

2. The flip chip package of claim 1 wherein the bump is constructed of a material selected to provide low yield strength, high ductility, and an oxidation- and corrosion-resistant bump surface.

3. The flip chip package of claim 2 wherein the bumps are formed of gold or a gold alloy.

4. The flip chip package of claim 1 wherein the bumps are formed on the input/output pads of the integrated circuit chip by a stud bumping process.

5. The flip chip package of claim 1 wherein the bumps are formed on the input/output pads of the integrated circuit chip by a solder bumping process.

6. The flip chip package of claim 1 wherein the bumps are formed on the input/output pads of the integrated circuit chip by an electroplating process.

7. A method for forming a flip chip package, comprising

providing an integrated circuit chip having interconnect bumps formed on input/output pads in a specified arrangement, each said interconnect bump having low yield strength, high ductility, and an oxidation- and corrosion-resistant surface;

providing a package substrate having a plurality of bond pads in an arrangement complementary to the specified arrangement of input/output pads on the integrated circuit chip;

contacting the bumps with the respective bond pads on the package substrate; and

thermo-mechanically treating the bumps to form solid-state connections of the bumps with their respective bond pads.

8. The method of claim 7 wherein the thermo-mechanically treating step comprises concurrently forcing the bump against the pad and heating the bump and pad.

9. A flip chip package, comprising

an integrated circuit chip having interconnect bumps formed on input/output pads in a specified arrangement in a surface thereof, and a package substrate having a plurality of bond pads in a complementary arrangement in a subjacent surface of the package substrate, wherein

second level interconnect sites are arranged in a second surface of the package substrate, and second level interconnect structures are connected to the respective second level interconnect sites, and wherein

a fill volume is defined between the integrated circuit chip and the package substrate, the fill volume being at least partly filled with at least one fill material, each said fill material having a selected specific elastic modulus, wherein regions of the fill volume that overlie the second level interconnect sites contain a lower specific elastic modulus fill material.

10. The flip chip package of claim 9 wherein the fill volume includes a first fill zone comprising a plurality of generally columnar volumes, generally overlying the plurality of second level interconnect sites; and the second fill zone consists of the remainder of the fill volume.

11. The flip chip package of claim 10 wherein at least a part of the first fill zone contains a first material having a lower specific elastic modulus, and at least a part of the second fill zone contains a second material having a higher specific elastic modulus.

12. The flip chip package of claim 11 wherein the first fill material has a specific elastic modulus less than about 0.5 GPa.

13. The flip chip package of claim 11 wherein the second fill material has a specific elastic modulus greater than about 5 GPa.

14. The flip chip package of claim 13 wherein the second fill material has a specific elastic modulus in a range about 5 GPa to about 15 GPa.

15. The flip chip package of claim 11 wherein the second fill material comprises an epoxy.

16. The flip chip package of claim 15 wherein the second fill material comprises an anhydride curable epoxy.

17. The flip chip package of claim 11 wherein the first fill zone comprises voids in the fill material within the fill volume.

18. The flip chip package of claim 11 wherein the first fill material comprises an adhesive.

19. The flip chip package of claim 18 wherein the first fill material comprises a silicon adhesive.

20. A method for making a flip chip package configured for interconnection to a printed circuit board, comprising

providing an integrated circuit chip having a surface;

providing a package substrate having a first surface and a second surface, the second surface being provided with a plurality of second level interconnect sites, the locations of the second level interconnect sites defining a plurality of first fill zone areas over the first surface of the package substrate, the remainder of the first surface of the package substrate constituting a second fill zone area;

dispensing at least a second fill material, having a specific elastic modulus greater than about 5 GPa, within the second fill zone area on the first surface of the package substrate; and

assembling the integrated circuit chip and the package substrate so that the second fill material is confined in a second fill zone within a volume defined between the integrated circuit chip surface and the first surface of the package substrate.

21. The method of claim 20 wherein the second fill material has a specific elastic modulus in a range about 5 GPa to about 15 GPa.

22. The method of claim 20, further comprising, prior to assembling the package, dispensing a first fill material having a specific elastic modulus less than about 0.5 GPa within the first fill zone area on the first surface of the package substrate.